

**REMARKS**

By the present amendment and response, independent claims 1 and 14 and dependent claim 17 have been amended to overcome the Examiner's objections and claim 16 has been canceled. Thus, claims 1-15 and 17- 25 are pending in the present application. Reconsideration and allowance of pending claims 1-15 and 17-25 in view of the following remarks are requested.

The Examiner has objected to claims 1, 9, 12, 20, and 23 because of informalities. In particular, the Examiner has stated that the singular term "region" in claim 1 should be replaced with the plural term "regions." Applicant respectfully submits that the singular term "region" in claim 1 is grammatically correct and, furthermore, the singular term "region" is an intended element in claim 1.

The Examiner has further objected to the use of a "\*" symbol in claims 9, 12, 20, and 23 to indicate a multiplication operation. Accordingly, the Examiner has stated that the "\*" symbol in claims 9, 12, 20, and 23 should be replaced with an "x" to indicate a multiplication operation. Applicant respectfully submits that the "\*" symbol is a well-known symbol that is commonly used to indicate a multiplication operation.

The Examiner has rejected claims 1, 3, 6-12, and 14-23 under 35 USC §102(b) as being anticipated by U.S. patent number 5,436,177 to Chiara Zaccherini ("Zaccherini"). Applicant respectfully submits that the present invention is patentably distinguishable over Zaccherini.

Initially, Applicant notes that the present invention is directed to economical and simplified fabrication of high resistivity resistors having improved temperature coefficients and more accurate control of resistivity values which are compatible with the formation of transistor gates in integrated CMOS processes. As disclosed in the present application, conventional methods utilized to fabricate a resistor and a transistor gate on a substrate in a CMOS process result in either a low resistivity resistor or require more than one masking step. See, for example, "prior art" FIG. 1A and related discussion in the background section of the present application. To overcome the above undesirable shortcomings of conventional methods, the present application discloses in detail the fabrication of a high resistivity resistor and a transistor gate on a substrate by a method comprising steps of forming a layer over a transistor gate and a field oxide region, forming a mask, i.e. a doping barrier, above the field oxide region of the layer, overdoping the layer over the transistor gate with a first dopant, removing the mask, and doping the layer over the transistor gate and the field oxide region with a second dopant so as to form a high resistivity resistor in the layer over the field oxide region. The layer over the transistor gate is overdoped with a first dopant to compensate for a subsequent doping of the layer with a second dopant such that the performance of a transistor comprising the transistor gate, such as a PFET, will be unaffected by the second dopant. See, for example, Figure 2 and the flow chart of Figure 3 and their related detailed descriptions. Thus, the present invention advantageously achieves fabrication of a high resistivity resistor and a transistor gate in a CMOS process, where the fabrication of the

polycrystalline layer 7 comprise a medium to low dosage, e.g. between  $1 \times 10^{12}$  and  $1 \times 10^{15}$  ions/cm<sup>2</sup>, of P-type dopant.

The present invention, as defined by amended independent claim 1, defines a method of forming a high resistivity resistor in a layer over a field oxide region, where the layer is also over a transistor gate, by overdoping the layer over the transistor gate with a first dopant while masking the layer over the field oxide region, and then removing the mask, i.e. the doping barrier, and doping the layer over the transistor gate and the field oxide region with a second dopant. In contrast and as described above, Zaccherini teaches away from forming a high resistivity resistor in a layer over a field oxide region, since Zaccherini discloses a wide range of doping dosages, e.g. between  $5 \times 10^{14}$  and  $1 \times 10^{16}$  ions/cm<sup>2</sup>, of N-type implant over channel region 4 and a medium to low dosage, e.g. between  $1 \times 10^{12}$  and  $1 \times 10^{15}$  ions/cm<sup>2</sup>, of P-type dopant to form a resistor in areas 8, i.e. field oxide regions, of polycrystalline layer 7. As such, the invention as defined by amended independent claim 1 is patentably distinguishable over Zaccherini.

Moreover, amended independent claim 14 of the present application defines a method of forming a high resistivity resistor in a polycrystalline silicon layer over a resistor region on a chip, where the polycrystalline silicon layer is also over a gate region, by overdoping the polycrystalline silicon layer over the gate region with a first dopant while masking the polycrystalline silicon layer over the resistor region, and then removing the mask, i.e. the doping barrier, and doping the polycrystalline silicon layer over the gate region and the transistor region with a second dopant. For the same reasons as discussed

above, the invention as defined by amended independent 14 is also patentably distinguishable over Zaccherini.

The Examiner has also rejected claims 2, 4-5, 13, and 24-25 as being unpatentable over Zaccherini in view of U.S. patent number 6,165,861 to Liu et al. ("Liu"). As discussed above, amended independent claims 1 and 14 are patentably distinguishable over Zaccherini and, as such, claims 2, 4-5, and 13 depending from amended independent claim 1 and claims 24-25 depending from amended independent claim 14 are, a fortiori, also patentably distinguishable over Zaccherini. Moreover, the features of amended independent claims 1 and 14, for example, forming a high resistivity resistor in a layer over a field oxide region or resistor region, where the layer is also over a transistor gate or gate region, and utilizing a single mask to form the high resistivity resistor, are not suggested, disclosed, or taught anywhere in Liu. As such, amended independent claim 1 and dependent claims 2, 4-5, and 13, and amended independent claim 14 and dependent claims 24-25 are also patentably distinguishable over Zaccherini in combination with Liu.

Thus, claims 1-15 and 17-25 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-15 and 17-25 pending in the present application is respectfully requested.

Respectfully Submitted,  
FARJAMI & FARJAMI LLP

Date: 7/12/02

  
Michael Farjami, Esq.  
Reg. No. 38, 135

Michael Farjami, Esq.  
FARJAMI & FARJAMI LLP  
16148 Sand Canyon  
Irvine, California 92618  
Telephone: (949) 784-4600  
Facsimile: (949) 784-4601

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed. Commissioner of Patents and Trademarks, Washington, D.C. 20231

Date of Deposit: 7-12-02

Lee Alme  
Name of Person Mailing Paper and or Fee

Ki Hu 7-12-02  
Signature Date